## REMARKS/ARGUMENTS

Amendment to the Specification

The specification has been amended to provide cross-references to related co-pending applications, which were inadvertently omitted at the time of filing.

Information Disclosure Statement (IDS)

Submitted herewith as a separate paper is an IDS citing all of the prior art references cited in the related application (U.S. Patent Application No. 09/982,459) but not cited in the present application. The IDS also cites prior art cited in an International Search Report (ISR) issued to a PCT application based on the present application.

Also submitted herewith as attachment for the Examiner's information is a copy of the Office Actions dated June 19, 2002, October 3, 2002, April 8, 2003, and January 13, 2004 in the U.S. Patent Application No. 09/982,459.

Applicants hereby respectfully request early consideration and acknowledgement of the prior art references cited in the IDS.

Claim Status and Amendment to the Claims

Claims 1-77 are now pending. No claims stand allowed.

Claims 1, 16, 31, 43, 58, 63, 68, and 73 have been amended to further particularly point out and distinctly claim subject matter regarded as the invention. The text of claims 2-15, 17-30, 32-42, 44-57, 59-62, 64-67, 69-72, and 74-77 is unchanged, but their

meaning is changed because they depend from amended claims. The amendment also contains minor changes of a clerical nature.

No "new matter" has been added by the amendment.

Amendment to Drawings

FIGS. 1-5 have been amended to be labeled as "PRIOR ART".

The 35 U.S.C. § 103 Rejection

Claims 1-77 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Camporese et al. (U.S. Pat. No. 6,205,571) and Graef (U.S. Pat. No. 6,305,001), among which claims 1, 16, 31, 43, 58, 63, 68, and 73 are independent claims. This rejection is respectfully traversed.

According to M.P.E.P. § 2143,

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in the applicant's disclosure.

Claim 1 defines a method of determining clock insertion delays for a microprocessor design having a grid-based clock distribution net. The claimed method comprises (a) partitioning the complete grid-based clock distribution net into a global clock net and a plurality of local clock nets, (b) simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global

clock net, said simulating including measuring clock arrival time and slope at each point where a clock element is connected, (c) simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets, and (d) combining the plurality of simulations to form a complete clock net simulation, as recited in claim 1 as amended.

Camporese allegedly discloses a grid tree clock distribution system which includes a first level tree wiring network **201**, a second level tree wires **203**, and an X-Y grid **204** as shown in FIG. 6 thereof. Camporese calculates all capacitance loads at grid intersection points of the X-Y grid-tree (column 7, lines 13-27 thereof), and lumped capacitances placed at the grid intersection points (column 11, lines 10-14 thereof). However, since Camporese focuses on approximation of various clock loads, all effects of the neighboring sectors are represented by the clustered grid loads (see ABSTRACT thereof). Thus, Camporese's simulation is only X-Y grid based (see FIGS. 9-10 thereof), and does not measure or observe the clock skew at specific points where clock elements are connected. Such measuring at specific points is also contrary to Camporese's clustering and smoothing of the clock loads. In addition, Camporese does not mention "clock slope" at all. Accordingly, Camporese fails to teach or suggest measuring, in local clock net simulation, clock arrival time and slope at each point where a clock element is connected, as recited in claim 1.

Graef allegedly teaches planning of the clock distribution network involving partitioning groups. However, similarly to Camporese, Graef also fails to teach or

suggest measuring clock arrival time and slope at points where a local clock net is connected to the global clock net, as claimed in claim 1.

Accordingly, Camporese, whether considered alone or combined with or modified by Graef, does not teach or suggest the claimed invention. Claims 16, 31, 43, 58, 63, 68, and 73 include substantially the same distinctive feature as claim 1. Thus, it is respectfully requested that the rejection of the claims based on Camporese and Graef be withdrawn.

In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

Dependent Claims

Claims 2-15 depend from claim 1, claims 17-30 depend from claim 16, claims 32-42 depend from claim 31, claims 44-57 depend from claim 43, claims 59-62 depend from claim 58, claims 64-67 depend from claim 63, claims 69-72 depend from claim 68, and claims 74-77 depend from claim 73, and thus include the limitations of respective independent claims. The argument set forth above is equally applicable here. The base claims being allowable, the dependent claims must also be allowable at least for the same reasons.

In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

Request for Allowance

It is believed that this Amendment places the above-identified patent application into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited.

If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the number indicated below.

Respectfully submitted,
THELEN REID & PRIEST, LLP

Dated: May 17, 2004

Masako Ando
Limited Recognition under 37 CFR §10.9(b)

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**BEFORE THE OFFICE OF ENROLLMENT AND DISCIPLINE**
**UNITED STATE PATENT AND TRADEMARK OFFICE**

## LIMITED RECOGNITION UNDER 37 CFR § 10.9(b)

Masako Ando is hereby given limited recognition under 37 CFR § 10.9(b) as an employee of Thelen, Reid & Priest LLP to prepare and prosecute patent applications wherein the patent applicant is the client of Thelen, Reid & Priest LLP, and the attorney or agent of record in the applications is a registered practitioner who is a member of Thelen, Reid & Priest LLP. This limited recognition shall expire on the date appearing below, or when whichever of the following events first occurs prior to the date appearing below: (i) Masako Ando ceases to lawfully reside in the United States, (ii) Masako Ando's employment with Thelen, Reid & Priest LLP ceases or is terminated, or (iii) Masako Ando ceases to remain or reside in the United States on an H-1 visa.

This document constitutes proof of such recognition. The original of this document is on file in the Office of Enrollment and Discipline of the U.S. Patent and Trademark Office.

**Expires: August 27, 2004**

Harry I. Moatz
Director of Enrollment and Discipline

UNITED STATES PATENT AND TRADEMARK OFFICE

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/982,459 | 10/17/2001 | Ralf Schmitt | SUN-P5405 | 7393 |

7590 01/13/2004

David B. Ritchie
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San Jose, CA 95164-0640



| EXAMINER | |
|---|---|
| THOMPSON, ANNETTE M | |
| ART UNIT | PAPER NUMBER |
| 2825 | |

DATE MAILED: 01/13/2004

Dkt'g + Final OA 3-13-04
APP 4-13-04
LD 7-13-04

Please find below and/or attached an Office communication concerning this application or proceeding.

IDS 8-28-03 ✓

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/982,459 | SCHMITT ET AL. | |
| | Examiner | Art Unit | |
| | A. M. Thompson | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 July 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-26* is/are allowed.

6)☒ Claim(s) *1-20 and 27-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *08/28/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

Applicants' Amendments to the Claims has been examined. Claims 1, 15, 27, and 32 are amended. Claims 1-36 are pending.

1. Applicants' Amendment is persuasive but introduces new rejections detailed, supra.

### *Drawings*

2. Figures 1-5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance. Also see the Notice of Draftperson's Patent Drawing Review of 06/19/2002.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 1-20 and 27-36** are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Pursuant to claims 1 and 15, these claims reference *storing clock arrival time and slope*. However, the generation, existence, or purpose of clock arrival times and slopes have not been established apriori, therefore this limitation lacks the required functional/structural cooperative relationship with the remaining claimed limitations. Claims dependent from claims 1 and 15 are likewise rejected.

***Allowable Subject Matter***

5. Claims 21-26 are allowed.

6. Claims 1 and 15 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

***Remarks***

7. Although Applicants' amendment is persuasive, new rejections necessitated by Applicant's amendment are introduced herein.

***Conclusion***

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications should be directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The

Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (571) 272-1907.

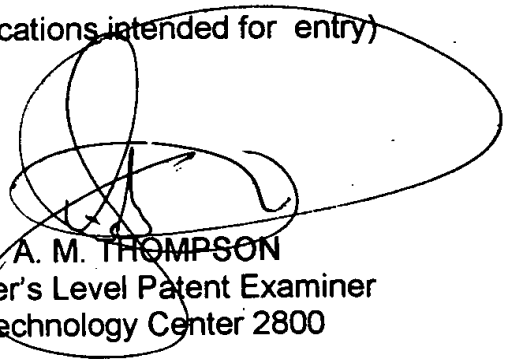
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-1562 or the Customer Service Center whose telephone number is (571) 272-1750.

10. Responses to this action should be mailed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for all **OFFICIAL** communications intended for entry)



A. M. THOMPSON
Master's Level Patent Examiner
Technology Center 2800

8/25/03





Form PTO 1449 (Rev. 2-32)

U.S. Department of Commerce
Patent and Trademark Office

| Atty. Docket No. | Serial No. |
|---|---|
| SUN-P5405 | 09/982,459 |

Applicant: Ralf M. Schmitt, et al.

**Information Disclosure Statement by Applicant**

Filed: October 17, 2001 Group: 2825

(Use several sheets if necessary)

**U.S. Patent Documents**

| Init. | | Document No. | Date | Name | Class | Subclass | Filing Date |
|---|---|---|---|---|---|---|---|
| | A | 6,053,950 | 4/25/00 | Shinagawa | 716 | 2 | 2/13/98 |
| | B | 6,150,865 | 11/21/00 | Fluxman et al. | 327 | 292 | 7/9/99 |
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**Foreign Documents**

| Init. | | Document No. | Date | Country | Class | Subclass | Translation Yes | Translation No |
|---|---|---|---|---|---|---|---|---|
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**Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)**

| | | |
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Examiner: _____ Date Considered: 8 January 2004

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.

811173-73
DBR/WEW

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/982,459 | 10/17/2001 | Ralf Schmitt | SUN-P5405 | 7393 |

7590 04/08/2003

David B. Ritchie
Thelen Reid & Priest LLP
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San Jose, CA 95164-0640



| EXAMINER |
|---|
| THOMPSON, ANNETTE M |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 04/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Mail log_____ Date_____

CPI sl Date 4/17/03

Excel_____ Date_____

| Office Action Summary | Application No. 09/982,459 | Applicant(s) SCHMITT ET AL. | |
|---|---|---|---|
| | Examiner A. M. Thompson | Art Unit 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-26* is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *27-36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

Applicants' Amendment and Response to Final Office Action has been examined. Claims 1, 7, 10, 15, 20, 21, and 26 are amended. Claims 27-36 are added. Claims 1-36 are pending.

### *Continued Examination Under 37 CFR 1.114*

1. A Request for Continued Examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8 January 2003 has been entered.

### *Claim Rejections - 35 USC § 103*

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Rejection of Claims 1-20**

4. **Claims 1-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Camporese et al. ("Camporese"), U.S. Patent 6,205,571 and Graef, U.S. Patent 6,305,001. Camporese discloses a clock tree distribution network for distributing a clock signal across a chip involving clock skew analysis. Although Camporese suggests Applicants' limitations, Camporese does not disclose a specific system for implementing the method. Graef also discloses a clock tree distribution planning method and additionally discloses a system for implementing the method that is a typical system used in IC designs. Graef further states that the system disclosed represents "one of many suitable computer platforms for implementing the method." (col. 15, ll. 47-50). Both Camporese and Graef disclose a method involving a clock distribution network.. However, Graef details the system that would be necessary to implement methods involving clock distribution networks in general. It therefore would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to use the system of Graef, or some similar system configuration, to implement the Camporese method.

5. Claims 15-18, 20, and 22-24 invoke the provisions of 35 U.S.C. 112, sixth paragraph and were considered accordingly.

6. Pursuant to claim 1 which recites a Clock Data Model (Fig. 2 illustrates this limitation; also, col. 3, ll. 48-50 discloses a clock-related electrical simulation model) for use with a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution comprising,

partitioning the complete clock net into a global clock net ( the first level wiring networks, e.g. Figure 2, #201; reference the Fig. 2 description at col. 4, ll. 25-28) and a plurality of local clock nets (the second level of tree wires, e.g. Figure 2, #203; reference the Figure 2 description at col. 4, ll. 28-31);

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net: col. 12, ll. 12-23 wherein the twig wiring represents the local clock nets; additionally, the $N_{sector}$ electrical lists comprise the loading for the plurality of local clock nets; simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets: col. 12, ll. 12-23 wherein the twig wiring represents the local clock nets; combining the plurality of simulations to form the complete clock net: col. 11, ll. 33-50; storing the plurality of simulations in the Clock Data Model: col. 11, ll. 19-22, wherein the tuned netlist represents the CDM with stored simulations, wherein the storing includes storing the simulated load for each point where the local clock net is connected to the global clock net (col. 11, ll. 10-14; col. 11, 19-26).

7. Pursuant to claim 2 wherein partitioning comprises breaking the complete clock net into equal sized parts according to rectangular grid coordinates: Figure 2 illustrates this limitation.

8. Pursuant to claim 3 wherein the method further comprises breaking at least one of the plurality of local clock nets down into at least one sub-local clock net: col. 4, ll. 28-31 suggests the existence of sub-local clock nets depending on the embodiment.

9. Pursuant to claim 4 wherein the method further comprises simulating the at least one sub-local clock net prior to simulating the corresponding local clock net: Fig. 7, step 735; col. 9, ll. 60-64.

10. Pursuant to claim 5 wherein at least two of the plurality of local clock nets are simulated in parallel: Creation of isolated net lists which represent local clock nets and are treated in parallel for tuning or simulation purposes, col. 9, ll. 8-27; see also col. 9, ll. 61-67 which discloses parallel tuning or simulation.

11. Pursuant to claim 6, wherein simulating the clock nets comprises extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database: the creation of the electrical netlist suggests this limitation, col. 6, ll. 10-65;

extracting component values of the elements of the local clock net from the microprocessor network database: col. 6, ll. 48-65;

simulating the local clock net based on the layout and the component values: col. 6, ll. 48-65;

extracting a load of the local clock net on the global clock net: col. 6, ll. 48-65.

12. Pursuant to claim 7 wherein simulating the local clock net comprises assuming that the clock arrival times form the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net: col. 9, ll. 35-43.

13. Pursuant to claim 8 wherein simulating the global clock net comprises extracting the layout of the global clock net from a microprocessor network database: the creation of the electrical netlist, col. 6, ll. 10-65, details the layout connections;

extracting component values of the elements of the global clock from the microprocessor network database: col. 6, ll. 48-65;

inserting the simulated loads of the plurality of local clock nets: col. 6, ll. 48-54; see also col. 7, ll. 13-15;

simulating the global clock net based on the layout, the component values, and the simulated local clock net loads: col. 6, ll. 48-65.

14. Pursuant to claim 9 which further comprises evaluating the complete clock net to determine whether the results converge: col. 9, ll. 35-60, wherein the true point load response matrix is checked against the smoothed point load response matrix which has calculations of clock signal arrival times.

15. Pursuant to claim 10 wherein if the results do not converge, setting the clock arrival times to those calculated for the simulated global clock net: col. 9, lines 47-56;

re-simulating one of the plurality of local clock nets to generate a load for the local and global clock net: col. 12, ll. 12-23;

re-simulating the global clock net based at least on the simulated or re-simulated load of each of the plurality of local clock nets: col. 12, ll. 12-13 wherein the twig wiring represents the local clock nets.

combining the simulations and re-simulations to form the complete net: col. 11, ll. 33-50.

16. Pursuant to claim 11, wherein re-simulating the local clock net comprises re-simulating the local clock net based on the layout, the component values, and the calculated clock arrival times: col. 6, ll. 48-65;

extracting a load of the at least one local clock net on the global clock net: col. 6, ll. 48-65.

17. Pursuant to claim 12 wherein the method comprises re-simulating at least a second of the plurality of local clock nets in parallel with the at least one local clock net:

18. Pursuant to claim 13, wherein re-simulating the global clock net comprises inserting the simulated or re-simulated loads of the plurality of local clock nets (col. 6, ll. 48-54; see also col. 7, ll. 13-15;) and

re-simulating the global clock net based on the layout, the component values, and the simulated or re-simulated local clock net loads: col. 6, ll. 48-65.

19. Pursuant to claim 14, wherein the method further comprises storing the plurality of re-simulations in the Clock Data Model: col. 11, ll. 19-22.

20. Pursuant to Claim 15 which recites [a] Clock Data Model for use with a system for determining clock insertion delays for a microprocessor design having grid-based distribution, the system comprising means for partitioning the complete clock net into a global clock net and a plurality of local clock nets, means for simulating each of the plurality of local clock nets on the global clock net, means for simulating the global clock net based on the simulated load of each of the plurality of local clock nets and means for combining the plurality of simulations to form the complete clock net, the CDM comprising means for storing the simulation results (Graef discloses a system having all the ("means for")elements of this limitation at col. 15, line 42 to col. 17, line 4); wherein the means for storing the simulated load for each point is where the local clock net is connected to the global clock net (Camporese, col. 11, ll. 10-14; col. 11, 19-26)

21. Pursuant to claim 16 further comprising means for collecting all of the information created during the plurality of simulations: Graef, col. 16, ll. 19-37.

22. Pursuant to claim 17 further comprising means for retrieving all of the information created during the plurality of simulations: Graef, col. 16, ll. 48-53.

23. Pursuant to claim 18 further comprising means for querying all of the information created during the plurality of simulations: col. 16, ll. 38-47.

24. Pursuant to claim 19 further comprising a timing tool interface to provide accurate clock arrival times for each clocked element in the microprocessor design: col. 16, ll. 1-5.

25. Pursuant to claim 20 wherein the system further comprises means for evaluating the complete clock net to determine whether the results converge (col. 9, ll. 35-60), means for *determining* that clock arrival times are those calculated for the simulated global clock net, means for re-simulating at least one of the plurality of local clock nets to generate a load for at least one local clock net on the global clock net, means for simulating the global clock net based on the simulated or re-simulated load of each of the plurality of local clock nets, and means for combining the simulations and re-simulations to form the complete clock net and wherein the CDM further comprises means for storing the plurality of re-simulation results (Graef discloses a system having all the ("means for") elements of this limitation at col. 15, line 42 to col. 17, line 4).

***Allowable Subject Matter***

26. Claims 21-26 are allowed.

27. Claims 27-36 contain allowable subject matter.

***28.*** The following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose a system for determining clock insertion delays for a microprocessor design with grid-based clock distribution that includes a local clock net simulator and global clock net simulator, a merging unit and a convergence evaluator unit. Further the prior art does not disclose a CDM as claimed wherein the clock arrival time and slope are stored for each point where the local clock net is connected to the global clock net.

***Remarks***

29. In this continued examination, Camporese at least suggests the added claim limitations. Therefore, the rejection of claims 1-20 under 35 U.S.C. 103(a) is sustained, herein, supra.

***Conclusion***

30. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to A.M. Thompson whose telephone number is (703) 305-7441. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 5:00 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (703) 308-1323.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956 or the Customer Service Center whose telephone number is (703)306-3329.

31. Responses to this action should be mailed to:

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or faxed to:

(703) 872-9318, (for **OFFICIAL** communications intended for entry)
(703)872-9319, (for Official **AFTER-FINAL** communications)

Hand-delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).

A. M. THOMPSON
Patent Examiner

7 April 2003

UNITED STATES PATENT AND TRADEMARK OFFICE

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/982,459 | 10/17/2001 | Ralf Schmitt | SUN-P5405 | 7393 |

7590 10/03/2002

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| EXAMINER | |
|---|---|
| THOMPSON, ANNETTE M | |
| ART UNIT | PAPER NUMBER |
| 2825 | |

DATE MAILED: 10/03/2002

OCT 10 2002

Please find below and/or attached an Office communication concerning this application or proceeding.

CPI
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PTO-90C (Rev. 07-01)

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/982,459 | SCHMITT ET AL. | |
| | Examiner | Art Unit | |
| | A. M. Thompson | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

Applicants' Amendment to 09/982,459, has been examined along with a review of the accompanying remarks. The specification is amended. Claims 1, 7-10, 15, 20, 21 and 26 are amended. Claims 1-26 are pending.

1. Applicants' Amendment is considered persuasive in part. The applicable objections and rejections from the prior non-final office action (Paper no. 3) are incorporated herein.

### *Claim Objections*

2. **Claims 7, 20, and 26** are objected to because of the following: Pursuant to claims 7 and 20, at line 2, the word "assuming" denotes uncertainty. Examiner suggests use of the word *determining* in lieu of assuming. Pursuant to claim 26, at line 3, the word "assumes" denotes uncertainty. Examiner suggests use of the word *determines* in lieu of assuming. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the **second paragraph** of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Pursuant to claims 1, 10, 15, 20, 21, and 26, they recite the limitation of *simulating the global clock net based in part on the simulated load of the plurality of clock nets*. However, Applicants' specification at page 14, lines 2-4, precisely states that the simulation is based on the layout, the component values and

the simulated clock net loads. Applicants should precisely claim the limitation based on the information in the specification instead of providing the partial recitation. All remaining claims (**2-7, 9, 11-14, 16-19, 22-25**), not specifically rejected here, are also rejected under this code section because they depend from rejected independent claims 1, 15, or 21.

***Claim Rejections - 35 USC § 103***

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Rejection of Claims 1-20**

7. **Claims 1-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Camporese et al. ("Camporese"), U.S. Patent 6,205,571 and Graef, U.S. Patent 6,305,001. Camporese discloses a clock tree distribution network for distributing a

clock signal across a chip involving clock skew analysis. Although Camporese suggests Applicants' limitations, Camporese does not disclose a specific system for implementing the method. Graef also discloses a clock tree distribution planning method and additionally discloses a system for implementing the method that is a typical system used in IC designs. Graef further states that the system disclosed represents "one of many suitable computer platforms for implementing the method." (col. 15, ll. 47-50). Both Camporese and Graef disclose a method involving a clock distribution network.. However, Graef details the system that would be necessary to implement methods involving clock distribution networks in general. It therefore would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to use the system of Graef, or some similar system configuration, to implement the Camporese method.

8. Claims 15-18, 20, and 22-24 invoke the provisions of 35 U.S.C. 112, sixth paragraph and were considered accordingly.

← camporese

9. Pursuant to claim 1 which recites a Clock Data Model (Fig. 2 illustrates this limitation; also, col. 3, ll. 48-50 discloses a clock-related electrical simulation model) for use with a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution comprising,

partitioning the complete clock net into a global clock net ( the first level wiring networks, e.g. Figure 2, #201; reference the Fig. 2 description at col. 4, ll. 25-28) and a plurality of local clock nets (the second level of tree wires, e.g. Figure 2, #203; reference the Figure 2 description at col. 4, ll. 28-31);

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net: col. 12, ll. 12-23 wherein the twig wiring represents the local clock nets; additionally, the $N_{sector}$ electrical lists comprise the loading for the plurality of local clock nets;.

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets: col. 12, ll. 12-23 wherein the twig wiring represents the local clock nets;

combining the plurality of simulations to form the complete clock net: col. 11, ll. 33-50;

storing the plurality of simulations in the Clock Data Model: col. 11, ll. 19-22, wherein the tuned netlist represents the CDM with stored simulations.

10. Pursuant to claim 2 wherein partitioning comprises breaking the complete clock net into equal sized parts according to rectangular grid coordinates: Figure 2 illustrates this limitation.

11. Pursuant to claim 3 wherein the method further comprises breaking at least one of the plurality of local clock nets down into at least one sub-local clock net: col. 4, ll. 28-31 suggests the existence of sub-local clock nets depending on the embodiment.

12. Pursuant to claim 4 wherein the method further comprises simulating the at least one sub-local clock net prior to simulating the corresponding local clock net: Fig. 7, step 735; col. 9, ll. 60-64.

13. Pursuant to claim 5 wherein at least two of the plurality of local clock nets are simulated in parallel: Creation of isolated net lists which represent local clock nets and

are treated in parallel for tuning or simulation purposes, col. 9, ll. 8-27; see also col. 9, ll. 61-67 which discloses parallel tuning or simulation.

14. Pursuant to claim 6, wherein simulating the clock nets comprises extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database: the creation of the electrical netlist suggests this limitation, col. 6, ll. 10-65;

extracting component values of the elements of the local clock net from the microprocessor network database: col. 6, ll. 48-65;

simulating the local clock net based on the layout and the component values: col. 6, ll. 48-65;

extracting a load of the local clock net on the global clock net: col. 6, ll. 48-65.

15. Pursuant to claim 7 wherein simulating the local clock net comprises assuming that the clock arrival times form the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net: col. 9, ll. 35-43.

16. Pursuant to claim 8 wherein simulating the global clock net comprises extracting the layout of the global clock net from a microprocessor network database: the creation of the electrical netlist, col. 6, ll. 10-65, details the layout connections;

extracting component values of the elements of the global clock from the microprocessor network database: col. 6, ll. 48-65;

inserting the simulated loads of the plurality of local clock nets: col. 6, ll. 48-54; see also col. 7, ll. 13-15;

simulating the global clock net based on the layout, the component values, and the simulated local clock net loads: col. 6, ll. 48-65.

17. Pursuant to claim 9 which further comprises evaluating the complete clock net to determine whether the results converge: col. 9, ll. 35-60, wherein the true point load response matrix is checked against the smoothed point load response matrix which has calculations of clock signal arrival times.

18. Pursuant to claim 10 wherein if the results do not converge, replacing the clock arrival times with those calculated for the simulated global clock net: col. 9, lines 47-56;

re-simulating one of the plurality of local clock nets to generate a load for the local and global clock net: col. 12, ll. 12-23;

re-simulating the global clock net based on the simulated or re-simulated load of each of the plurality of local clock nets: col. 12, ll. 12-13 wherein the twig wiring represents the local clock nets.

combining the simulations and re-simulations to form the complete net: col. 11, ll. 33-50.

19. Pursuant to claim 11, wherein re-simulating the local clock net comprises re-simulating the local clock net based on the layout, the component values, and the calculated clock arrival times: col. 6, ll. 48-65;

extracting a load of the at least one local clock net on the global clock net: col. 6, ll. 48-65.

20. Pursuant to claim 12 wherein the method comprises re-simulating at least a second of the plurality of local clock nets in parallel with the at least one local clock net:

21. Pursuant to claim 13, wherein re-simulating the global clock net comprises inserting the simulated or re-simulated loads of the plurality of local clock nets (col. 6, ll. 48-54; see also col. 7, ll. 13-15;) and

re-simulating the global clock net based on the layout, the component values, and the simulated or re-simulated local clock net loads: col. 6, ll. 48-65.

22. Pursuant to claim 14, wherein the method further comprises storing the plurality of re-simulations in the Clock Data Model: col. 11, ll. 19-22.

23. Pursuant to Claim 15 which recites [a] Clock Data Model for use with a system for determining clock insertion delays for a microprocessor design having grid-based distribution, the system comprising means for partitioning the complete clock net into a global clock net and a plurality of local clock nets, means for simulating each of the plurality of local clock nets on the global clock net, means for simulating the global clock net based on the simulated load of each of the plurality of local clock nets and means for combining the plurality of simulations to form the complete clock net, the CDM comprising means for storing the simulation results (Graef discloses a system having all the ("means for")elements of this limitation at col. 15, line 42 to col. 17, line 4).

24. Pursuant to claim 16 further comprising means for collecting all of the information created during the plurality of simulations: Graef, col. 16, ll. 19-37.

25. Pursuant to claim 17 further comprising means for retrieving all of the information created during the plurality of simulations: Graef, col. 16, ll. 48-53.

26. Pursuant to claim 18 further comprising means for querying all of the information created during the plurality of simulations: col. 16, ll. 38-47.

27. Pursuant to claim 19 further comprising a timing tool interface to provide accurate clock arrival times for each clocked element in the microprocessor design: col. 16, ll. 1-5.

28. Pursuant to claim 20 wherein the system further comprises means for evaluating the complete clock net to determine whether the results converge (col. 9, ll. 35-60), means for *determining* that clock arrival times are those calculated for the simulated global clock net, means for re-simulating at least one of the plurality of local clock nets to generate a load for at least one local clock net on the global clock net, means for simulating the global clock net based on the simulated or re-simulated load of each of the plurality of local clock nets, and means for combining the simulations and re-simulations to form the complete clock net and wherein the CDM further comprises means for storing the plurality of re-simulation results (Graef discloses a system having all the ("means for") elements of this limitation at col. 15, line 42 to col. 17, line 4).

***Allowable Subject Matter***

29. Claims 21-26 contain allowable subject matter.

30. Claim 21 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

31. Claims 22-26 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

32. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose a system for determining clock insertion delays for a microprocessor design with grid-based clock distribution that includes a local clock net simulator and global clock net simulator, a merging unit and a convergence evaluator unit.

***Remarks***

33. With respect to claims 7, 20, and 26, use of the word "assumes" in a specification is not the same as use of the word "assumes" in the claims. The claims are required to be definite, and use of the word assumes connotes uncertainity. Examiner has suggested at least one way for Applicants to overcome the problem. Another way could be to dispense with the use of the word "assumes" in the claims.

34. The 35 U.S.C 112, second paragraph, rejections are maintained because the metes and bounds of the phrase "in part" cannot be determined.

35. The 35 U.S.C. 103 rejections are maintained because despite Applicants' traversals, Applicants' claimed limitations are within the scope of the prior art applied. For example, Applicants claims "partitioning a complete clock net into a global clock net and a plurality of local clock nets." Examiner referenced Camporese Figure 2, #201, for the global clock net and Camporese Figure 2, #203 for the local clock net. The levels cited in Camporese with respect to the global and local clock nets are similar to the levels cited in Applicants' specification, page 5, lines 20-24, to define the meaning of a global and local net. Contrary to Applicants' assertions, Examiner did not define the

meaning of Applicants' terms but rather looked to Applicants' specification to define the scope of the terms which in this case are encompassed by the prior art.

***Conclusion***

36. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

37. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to A.M. Thompson whose telephone number is (703) 305-7441. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 5:00 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (703) 308-1323.

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Hand-delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).

A. M. THOMPSON
Patent Examiner

VUTHE SIEK
PRIMARY EXAMINER

| Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office | Atty. Docket No. SUN-P5405 | Serial No. 09/982,459 |
|---|---|---|
| **Information Disclosure Statement by Applicant** | Applicant: Ralf M. Schmitt, et al. | |
| (Use several sheets if necessary) | Filed: October 17, 2001 | Group: 2825 |

**U.S. Patent Documents**

| Init. | | Document No. | Date | Name | Class | Subclass | Filing Date |
|---|---|---|---|---|---|---|---|
| | A | 5,239,215 | 8/24/93 | Yamaguchi | 307 | 480 | 11/20/92 |
| | B | 6,150,865 | 11/21/00 | Fluxman et al. | 327 | 292 | 7/9/99 |
| | C | 6,311,313 | 10/30/01 | Camporese et al. | 716 | 6 | 12/29/98 |



**Foreign Documents**

| Init. | | Document No. | Date | Country | Class | Subclass | Translation Yes | Translation No |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| | | | | | | | | |

**Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)**

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| Examiner | Date Considered 28-Sept-2002 |
|---|---|

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.

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| Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office | Atty. Docket No. SUN-P5405 | Serial No. 09/982,459 |
|---|---|---|
| **Information Disclosure Statement by Applicant** (Use several sheets if necessary) | Applicant: Ralf M. Schmitt, et al. | |
| | Filed: October 17, 2001 | Group: 2825 |

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**U.S. Patent Documents**

| Init. | | Document No. | Date | Name | Class | Subclass | Filing Date |
|---|---|---|---|---|---|---|---|
| | A | 5,239,215 | 8/24/93 | Yamaguchi | 307 | 480 | 11/20/92 |
| | B | 6,150,865 | 11/21/00 | Fluxman et al. | 327 | 292 | 7/9/99 |
| | C | 6,311,313 | 10/30/01 | Camporese et al. | 716 | 6 | 12/29/98 |

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**Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)**

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| Examiner | Date Considered 28-Sept-2002 |
|---|---|

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**Quality Assurance Specialists:**
**Don Hajec.....703-308-4075** **Paul Dzierzynski.....703-308-4822**

If the contents of the attached correspondence have any clerical omissions, e.g., missing references or pages, illegible text, or any other similar errors, please contact us at the number below. We will take appropriate action to xpedite the necessary corrections. Also, if you have general questions concerning any application assigned t Technology Center 2800, please contact our Customer Service Center. Questions concerning the merits of the application must be directed to the Examiner in charge of the particular application, then to the supervisor if appropriate.

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| | | |
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| Sharon Gibson | 703/308-0658 | 2810 |
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| Richard Seidel | 703/306-343[illegible] | 2830/40 |
| Howard N Goldberg | 703/306-343[illegible] | 2850/60 |
| Janice A Falcone | 709/308-0530 | 2870/80 |

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/982,459 | 10/17/2001 | Ralf Schmitt | SUN-P5405 | 7393 |

7590 06/19/2002

David B. Ritchie
Thelen Reid & Priest LLP
P .O. Box 640640
San Jose, CA 95164-0640



| EXAMINER | |
|---|---|
| THOMPSON, ANNETTE M | |
| ART UNIT | PAPER NUMBER |
| 2825 | |

DATE MAILED: 06/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

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| EXAMINER | |
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| THOMPSON, ANNETTE M | |
| ART UNIT | PAPER NUMBER |
| 2825 | |

DATE MAILED: 06/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/982,459 | SCHMITT ET AL. | |
| | Examiner | Art Unit | |
| | A. M. Thompson | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

| Notice of References Cited | Application/Control No. 09/982,459 | Applicant(s)/Patent Under Reexamination SCHMITT ET AL. | |
|---|---|---|---|
| | Examiner A. M. Thompson | Art Unit 2825 | Page 1 of 2 |

**U.S. PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | Classification |
|---|---|---|---|---|---|
| | A | US-6,205,571 | 03-2001 | Camporese et al. | 716/2 |
| | B | US-6,305,001 | 10-2001 | Graef | 716/12 |
| | C | US-6,311,313 | 10-2001 | Camporese et al. | 716/6 |
| | D | US-5,387,885 | 02-1995 | Chi | 333/100 |
| | E | US-5,239,215 | 08-1993 | Yamaguchi | 307/480 |
| | F | US-5,656,963 | 08-1997 | Masleid et al. | 327/297 |
| | G | US-6,088,254 | 07-2000 | Kermani | 365/63 |
| | H | US-5,467,040 | 11-1995 | Nelson et al. | 327/276 |
| | I | US-6,150,865 | 11-2000 | Fluxman et al. | 327/292 |
| | J | US-6,025,740 | 02-2000 | Fukuyama | 326/93 |
| | K | US-6,204,713 | 03-2001 | Adams et al. | 327/295 |
| | L | US-5,923,188 | 07-1999 | Kametani et al. | 326/93 |
| | M | US-5,994,924 | 11-1999 | Lee et al. | 326/93 |

**FOREIGN PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Country | Name | Classification |
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**NON-PATENT DOCUMENTS**

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| | U | J. Burkis, Clock Tree Synthesis for High Performance ASICs, IEEE, page 9-8.1 - 9-8.3, August 1991. |
| | V | J-S Yim et al., A Floorplan-based Planning Methodology for Power and Clock Distribution in ASICs, Proceedings ACM/IEEE Conference on Design Automation, pages 766-771, June 1999. |
| | W | P.J. Restle et al., A Clock Distribution Network for Microprocessors, 2000 Symposium on VLSI Circuits, pages 184-187, April 2000. |
| | X | B. Lampson et al., A Processor for a High-Performance Personal Computer, Seventh Annual Symposium on Computer Architecture, pages 146-160, May 1980. |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

| Notice of References Cited | Application/Control No. 09/982,459 | Applicant(s)/Patent Under Reexamination SCHMITT ET AL. | |
|---|---|---|---|
| | Examiner A. M. Thompson | Art Unit 2825 | Page 2 of 2 |

**U.S. PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | Classification |
|---|---|---|---|---|---|
| | A | US-6,378,080 | 04-2000 | Anjo et al. | 713/500 |
| | B | US-6,053,950 | 04-2000 | Shinagawa | 716/12 |
| | C | US-5,896,055 | 04-1999 | Toyonaga et al. | 327/295 |
| | D | US-5,911,063 | 06-1999 | Allen et al. | 395/555 |
| | E | US- | | | |
| | F | US- | | | |
| | G | US- | | | |
| | H | US- | | | |
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| | M | US- | | | |

**FOREIGN PATENT DOCUMENTS**

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**NON-PATENT DOCUMENTS**

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| | U | C-S Wu et al., An Automatic Cell Characterization Environment for Cell-Based Design Methodology, IEEE, pages 326-329, May 1993. |
| | V | |
| | W | |
| | X | |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

## DETAILED ACTION

This application, 09/982,459, has been examined. Claims 1-26 are pending.

### *Specification*

1. The disclosure is objected to because of the following informalities: at page 14, line 18, correct spelling for *assess*. At page 13, line 6, change "thought" to *though*. Additionally, the specification states (e.g. at page 12, lines 4-5) combining the simulations to form a complete clock net. However, the specification should more accurately state that the simulations are combined to form a complete clock net *simulation*. Appropriate correction is required.

### *Claim Objections*

2. Claims 1, 7-10, 15, 20, 21, and 26 are objected to because of the following: Pursuant to claims 1, 10, 15, 20, 21, and 26 which recite *combining simulations to form a complete clock net*, Applicants must clarify that it is not the simulations which form a complete clock net, rather combining the simulations form the complete clock net simulation. The specification also requires similar clarification (e.g., page 12, lines 4-5). Pursuant to claims 7 and 20, at line 2, the word "assuming" denotes uncertainty. Examiner suggests use of the word *determining* in lieu of assuming. Pursuant to claim 26, at line 3, the word "assumes" denotes uncertainty. Examiner suggests use of the word *determines* in lieu of assuming. Pursuant to claim 8, at line 6, Applicants should indicate where the simulated loads are being inserted (into the database ?). Pursuant to claim 9, it is the simulation that is evaluated; so, after "complete clock net" insert - - simulation- -. Pursuant to claim 26, at lines 5 and lines 6, use the gerund form of "re-

1 9 10 15 20 21 26

simulate", i.e., *re-simulating;* at line 8, use the gerund form of "combines". Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the **second paragraph** of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 1-26** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Pursuant to **claims 1, 10, 15, 20, 21, and 26**, they recite the limitation of *simulating the global clock net based in part on the simulated load of the plurality of clock nets.* However, Applicants' specification at page 14, lines 2-4, precisely states that the simulation is based on the layout, the component values and the simulated clock net loads. Applicants should precisely claim the limitation based on the information in the specification instead of providing the partial recitation. Pursuant to **claim 8**, at line 3, "the layout" lacks antecedent basis. Additionally, pursuant to **claim 26**, at line 3, "the apparatus" lacks antecedent basis. All remaining claims (**2-7, 9, 11-14, 16-19, 22-25**), not specifically rejected here, are also rejected under this code section because they depend from rejected independent claims 1, 15, or 21.

5. **Claim 9** recites the limitation "the results" in line 2. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 103***

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Rejection of Claims 1-20**

8. **Claims 1-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Camporese et al. ("Camporese"), U.S. Patent 6,205,571 and Graef, U.S. Patent 6,305,001. Camporese discloses a clock tree distribution network for distributing a clock signal across a chip involving clock skew analysis. Although Camporese suggests Applicants' limitations, Camporese does not disclose a specific system for implementing the method. Graef also discloses a clock tree distribution planning method and additionally discloses a system for implementing the method that is a typical system used in IC designs. Graef further states that the system disclosed represents "one of many suitable computer platforms for implementing the method." (col. 15, ll. 47-50). Both Camporese and Graef disclose a method involving a clock distribution network.. However, Graef details the system that would be necessary to

implement methods involving clock distribution networks in general. It therefore would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to use the system of Graef, or some similar system configuration, to implement the Camporese method.

9. Claims 15-18, 20, and 22-24 invoke the provisions of 35 U.S.C. 112, sixth paragraph and were considered accordingly.

10. Pursuant to claim 1 which recites a Clock Data Model (Fig. 2 illustrates this limitation; also, col. 3, ll. 48-50 discloses a clock-related electrical simulation model) for use with a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution comprising,

partitioning the complete clock net into a global clock net ( the first level wiring networks, e.g. Figure 2, #201; reference the Fig. 2 description at col. 4, ll. 25-28) and a plurality of local clock nets (the second level of tree wires, e.g. Figure 2, #203; reference the Figure 2 description at col. 4, ll. 28-31);

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net: col. 12, ll. 12-23 wherein the twig wiring represents the local clock nets; additionally, the $N_{sector}$ electrical lists comprise the loading for the plurality of local clock nets;.

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets: col. 12, ll. 12-23 wherein the twig wiring represents the local clock nets;

combining the plurality of simulations to form the complete clock net: col. 11, ll. 33-50;

storing the plurality of simulations in the Clock Data Model: col. 11, ll. 19-22, wherein the tuned netlist represents the CDM with stored simulations.

11. Pursuant to claim 2 wherein partitioning comprises breaking the complete clock net into equal sized parts according to rectangular grid coordinates: Figure 2 illustrates this limitation.

12. Pursuant to claim 3 wherein the method further comprises breaking at least one of the plurality of local clock nets down into at least one sub-local clock net: col. 4, ll. 28-31 suggests the existence of sub-local clock nets depending on the embodiment.

13. Pursuant to claim 4 wherein the method further comprises simulating the at least one sub-local clock net prior to simulating the corresponding local clock net: Fig. 7, step 735; col. 9, ll. 60-64.

14. Pursuant to claim 5 wherein at least two of the plurality of local clock nets are simulated in parallel: Creation of isolated net lists which represent local clock nets and are treated in parallel for tuning or simulation purposes, col. 9, ll. 8-27; see also col. 9, ll. 61-67 which discloses parallel tuning or simulation.

15. Pursuant to claim 6, wherein simulating the clock nets comprises extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database: the creation of the electrical netlist suggests this limitation, col. 6, ll. 10-65;

extracting component values of the elements of the local clock net from the microprocessor network database: col. 6, ll. 48-65;

simulating the local clock net based on the layout and the component values: col. 6, ll. 48-65;

extracting a load of the local clock net on the global clock net: col. 6, ll. 48-65.

16. Pursuant to claim 7 wherein simulating the local clock net comprises assuming that the clock arrival times form the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net: col. 9, ll. 35-43.

17. Pursuant to claim 8 wherein simulating the global clock net comprises extracting the layout of the global clock net from a microprocessor network database: the creation of the electrical netlist, col. 6, ll. 10-65, details the layout connections;

extracting component values of the elements of the global clock from the microprocessor network database: col. 6, ll. 48-65;

inserting the simulated loads of the plurality of local clock nets: col. 6, ll. 48-54; see also col. 7, ll. 13-15;

simulating the global clock net based on the layout, the component values, and the simulated local clock net loads: col. 6, ll. 48-65.

18. Pursuant to claim 9 which further comprises evaluating the complete clock net to determine whether the results converge: col. 9, ll. 35-60, wherein the true point load response matrix is checked against the smoothed point load response matrix which has calculations of clock signal arrival times.

19. Pursuant to claim 10 wherein if the results do not converge, replacing the clock arrival times with those calculated for the simulated global clock net: col. 9, lines 47-56;

re-simulating one of the plurality of local clock nets to generate a load for the local and global clock net: col. 12, ll. 12-23;

re-simulating the global clock net based on the simulated or re-simulated load of each of the plurality of local clock nets: col. 12, ll. 12-13 wherein the twig wiring represents the local clock nets.

combining the simulations and re-simulations to form the complete net: col. 11, ll. 33-50.

20. Pursuant to claim 11, wherein re-simulating the local clock net comprises re-simulating the local clock net based on the layout, the component values, and the calculated clock arrival times: col. 6, ll. 48-65;

extracting a load of the at least one local clock net on the global clock net: col. 6, ll. 48-65.

21. Pursuant to claim 12 wherein the method comprises re-simulating at least a second of the plurality of local clock nets in parallel with the at least one local clock net:

22. Pursuant to claim 13, wherein re-simulating the global clock net comprises inserting the simulated or re-simulated loads of the plurality of local clock nets (col. 6, ll. 48-54; see also col. 7, ll. 13-15;) and

re-simulating the global clock net based on the layout, the component values, and the simulated or re-simulated local clock net loads: col. 6, ll. 48-65.

23. Pursuant to claim 14, wherein the method further comprises storing the plurality of re-simulations in the Clock Data Model: col. 11, ll. 19-22.

24. Pursuant to Claim 15 which recites [a] Clock Data Model for use with a system for determining clock insertion delays for a microprocessor design having grid-based distribution, the system comprising means for partitioning the complete clock net into a global clock net and a plurality of local clock nets, means for simulating each of the plurality of local clock nets on the global clock net, means for simulating the global clock net based on the simulated load of each of the plurality of local clock nets and means for combining the plurality of simulations to form the complete clock net, the CDM comprising means for storing the simulation results (Graef discloses a system having all the ("means for")elements of this limitation at col. 15, line 42 to col. 17, line 4).

25. Pursuant to claim 16 further comprising means for collecting all of the information created during the plurality of simulations: Graef, col. 16, ll. 19-37.

26. Pursuant to claim 17 further comprising means for retrieving all of the information created during the plurality of simulations: Graef, col. 16, ll. 48-53.

27. Pursuant to claim 18 further comprising means for querying all of the information created during the plurality of simulations: col. 16, ll. 38-47.

28. Pursuant to claim 19 further comprising a timing tool interface to provide accurate clock arrival times for each clocked element in the microprocessor design: col. 16, ll. 1-5.

29. Pursuant to claim 20 wherein the system further comprises means for evaluating the complete clock net to determine whether the results converge (col. 9, ll. 35-60), means for *determining* that clock arrival times are those calculated for the simulated global clock net, means for re-simulating at least one of the plurality of local clock nets

to generate a load for at least one local clock net on the global clock net, means for simulating the global clock net based on the simulated or re-simulated load of each of the plurality of local clock nets, and means for combining the simulations and re-simulations to form the complete clock net and wherein the CDM further comprises means for storing the plurality of re-simulation results (Graef discloses a system having all the ("means for") elements of this limitation at col. 15, line 42 to col. 17, line 4).

***Allowable Subject Matter***

30. Claims 21-26 contain allowable subject matter.

31. Claim 21 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

32. Claims 22-26 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

33. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose a system for determining clock insertion delays for a microprocessor design with grid-based clock distribution that includes a local clock net simulator and global clock net simulator, a merging unit and a convergence evaluator unit.

***Conclusion***

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Please refer to the PTO-892 for a complete listing.

35. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to A.M. Thompson whose telephone number is (703) 305-7441. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 5:00 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (703) 308-1323.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956 or the Customer Service Center whose telephone number is (703)306-3329.

Responses to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9318, (for **OFFICIAL** communications intended for entry)
(703)872-9319, (for Official **AFTER-FINAL** communications)

Hand-delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).

A. M. THOMPSON
Patent Examiner
June 17, 2002

| Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office | Atty. Docket No. SUN-P5405 | Serial No. 09/982,459 |
|---|---|---|
| **Information Disclosure Statement by Applicant** (Use several sheets if necessary) | Applicant: Ralf M. Schmitt, et al. | |
| | Filed: October 17, 2001 | Group: (to be assigned) |

**U.S. Patent Documents**

| Init. | | Document No. | Date | Name | Class | Subclass | Filing Date |
|---|---|---|---|---|---|---|---|
| | A | 5,911,063 | 6/8/99 | Allen et al. | 395 | 555 | 8/18/97 |
| | B | 5,923,188 | 7/13/99 | Kametani et al. | 326 | 93 | 6/12/96 |
| | C | 6,025,740 | 2/15/00 | Fukuyama | 326 | 93 | 9/3/93 |



**Foreign Documents**

| Init. | | Document No. | Date | Country | Class | Subclass | Translation Yes | Translation No |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |



**Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)**

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|---|---|---|
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Examiner: _____ Date Considered: 7-May-2002

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.

| Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office | Atty. Docket No. SUN-P5405 | Serial No. 09/982,459 |
|---|---|---|
| **Information Disclosure Statement by Applicant** (Use several sheets if necessary) | Applicant: Ralf M. Schmitt, et al. | |
| | Filed: October 17, 2001 | Group: (to be assigned) |

**U.S. Patent Documents**

| Init. | | Document No. | Date | Name | Class | Subclass | Filing Date |
|---|---|---|---|---|---|---|---|
| | A | 5,911,063 | 6/8/99 | Allen et al. | 395 | 555 | 8/18/97 |
| | B | 5,923,188 | 7/13/99 | Kametani et al. | 326 | 93 | 6/12/96 |
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**Foreign Documents**

| Init. | | Document No. | Date | Country | Class | Subclass | Translation Yes | Translation No |
|---|---|---|---|---|---|---|---|---|



**Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)**

| | | |
|---|---|---|

| Examiner | Date Considered 7-May-2002 |
|---|---|

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.

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